1. A method for enabling a processor that directs I/O requests over a first communications channel to a first plurality of logical devices and to switch and direct I/O requests over a second channel to a second plurality of logical devices normally operating as a mirror of the first plurality of logical devices wherein each of the plurality of logical devices has an identifying control block and the processor I/O requests normally are processed using control blocks for the first plurality of logical devices, said method comprising:

A) determining, during normal operations, an operating validity of the first and second pluralities of logical devices,

B) initiating an address switch by:

i) verifying the operating validity of the first and second pluralities of logical devices, and

ii) exchanging the information in each control block associated with the first plurality of logical devices with the information in each control block associated with the second plurality of logical devices whereby subsequent processor I/O requests are directed to the second plurality of logical devices.

2. A method as recited in claim 1 wherein said determination of operating validity occurs asynchronously and independently of said exchange of control block information.

3. A method as recited in claim 2 wherein said determination is made periodically.

4. A method as recited in claim 2 wherein the processor and logical devices can operate with different configurations and wherein said determination responds to a change in a configuration.

5. A method as recited in claim 2 wherein the processor and logical devices can operate in different operating modes, and wherein said determination responds to the selected operating mode of the process with the first plurality of logical devices.

6. A method as recited in claim 2 wherein said determination includes a determination of validity for each of the first plurality of logical devices and the corresponding logical device in the second plurality of logical devices.

7. A method as recited in claim 6 wherein a data structure includes a validity flag for each of the first plurality of logical devices and its corresponding one of the second plurality of logical devices and wherein said determination of validity sets the corresponding validity flag.

8. A method as recited in claim 7 wherein said exchange of information occurs while all the logical devices have been blocked for responding to any I/O request, said block being released after all the exchanges are made whereby the redirection of processor I/O requests to the second plurality of logical devices occur essentially simultaneously.

9. A method as recited in claim 7 wherein said exchange includes the steps of:

i) selecting a single logical device in the first plurality of logical devices,

ii) blocking access to that logical device,

iii) and thereafter exchanging the information in each control block associated with the selected one of the first plurality of logical devices

and the corresponding of the second plurality of logical devices; and

iv) unblocking access to the logical devices.

10. Apparatus for enabling a processor that directs I/O requests over a first communications channel to a first plurality of logical devices and to switch and direct I/O requests over a second channel to a second plurality of logical devices normally operating as a mirror of the first plurality of logical devices wherein each of the plurality of logical devices has an identifying control block and the processor I/O requests normally are processed using control blocks for the first plurality of logical devices, said method comprising:

A) means for determining, during normal operations, an operating validity of the first and second pluralities of logical devices,

B) means for initiating an address switch including:

i) means for verifying the operating validity of the first and second pluralities of logical devices, and

ii) means for exchanging the information in each control block associated with the first plurality of logical devices with the information in each control block associated with the second plurality of logical devices

whereby subsequent processor I/O requests are directed to the second plurality of logical devices.

11. Apparatus as recited in claim 10 additionally comprising means for activating said determination means asynchronously and independently of the operation of said exchange means.

12. Apparatus as recited in claim 11 additionally comprising means for activating said determination periodically.

13. Apparatus as recited in claim 11 wherein the processor and logical devices can operate with different configurations and wherein said apparatus additionally comprises means for activating said determination means in response to a configuration change.

14. Apparatus as recited in claim 11 wherein the processor and logical devices can operate in different operating modes, and wherein said apparatus additionally comprises means for activating said determination means in response to the selected operating mode of the process with the first plurality of logical devices.

15. Apparatus as recited in claim 11 wherein said determination means includes means for determining the validity for each of the first plurality of logical devices and the corresponding logical device in the second plurality of logical devices.

16. Apparatus as recited in claim 15 additionally comprising a data structure including a validity flag for each of the first plurality of logical devices and its corresponding one of the second plurality of logical devices, said determination means sets the corresponding validity flag if valid operating conditions exist.

17. Apparatus as recited in claim 16 additionally comprising means for blocking access to all the logical devices before the information exchanges and means for releasing said blocking means after all the exchanges are made whereby the redirection of processor I/O requests to the second plurality of logical devices occur essentially simultaneously.

18. Apparatus as recited in claim 16 wherein said exchange means includes:

i) means for selecting a single logical device in the first plurality of logical devices,

ii) means for blocking access to that logical device, said exchange means being activated in response to said blocking means, and

iii) means for releasing said unblocking means.